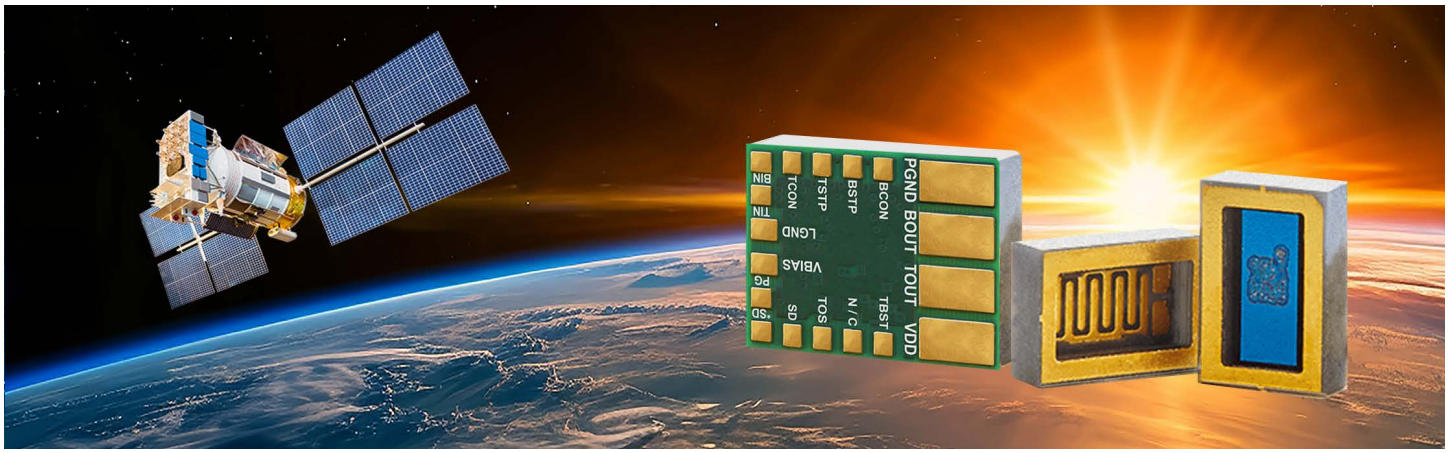
# Multiphase Interleaving Extends the Output Current/ Power and Versatility of the FBS-GAM02 and FBS-GAM02-PSE Modules




## Introduction

The FBS-GAM02 and GAM02-PSE modules provide the designer a high, density, rad hard solution for POL applications. But both these modules are limited in the output current that they can provide by themselves: The GAM02 is rated for 10 A and the GAM02-PSE can drive up to four (4) power HEMTs with individual ratings up to 50 A each. The latter may seem adequate for even the most demanding load, but thermal limitations and de-rating reduce the practical, individual current ratings for each HEMT to 25 A or less. This means that the maximum load current for a GAM02-PSE driving four discrete HEMTS is in the range of 100 A. Although possible, depending upon the thermal situation, parameter de-rating and PCB layout this may still be an aggressive current target.

This might seem like a dead end for the GAM02 series in terms of maximum output current that may be provided, but there is a design implementation/technique that allows for even higher currents to be provided by GAM02 or GAM02-PSE modules.

## Multiphase Interleaving

Multiphase interleaving of POL converters, see Figure 1 for an example using N primitive individual converter cells, is the technique whereby individual POL converters of lower ratings are paralleled as individual “phases” and that contribute equal current in time to a common load.

In Figure 1 the components Qc, Qs, Ds and the gate drivers/ level shift are representative of the GAM02 module or the GAM02-PSE module with external power HEMTs and catch Schottky.

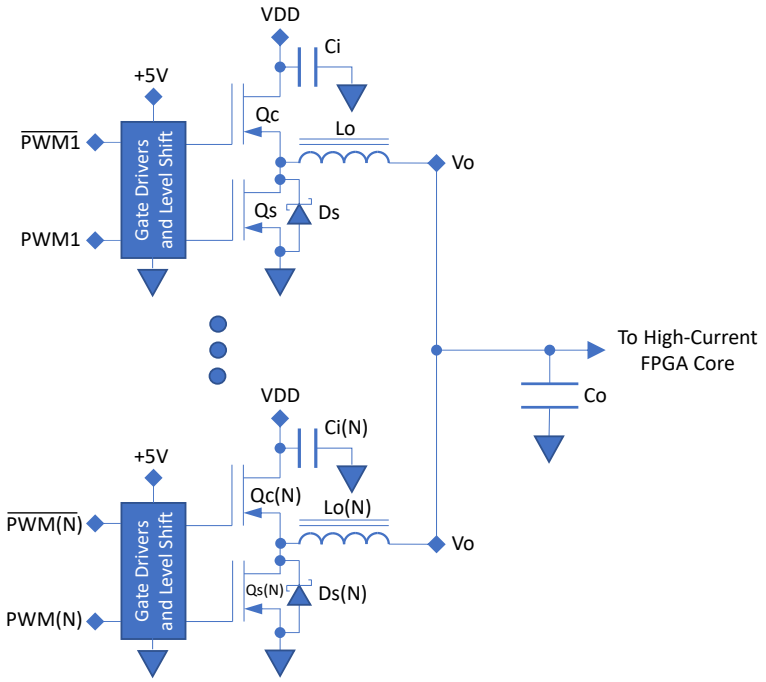



*Figure 1. Primitive Multiphase, Interleaved POL Converters*

In the most basic sense, this technique allows for N phases to be implemented by staggering (phase-shifting) the ON times (DT1… DTN) of each converter in time during a single switching cycle for each POL, as shown in Figure 2. Each phase provides current to the load during its ON time, allowing N times the current that may be provided by a single POL converter.

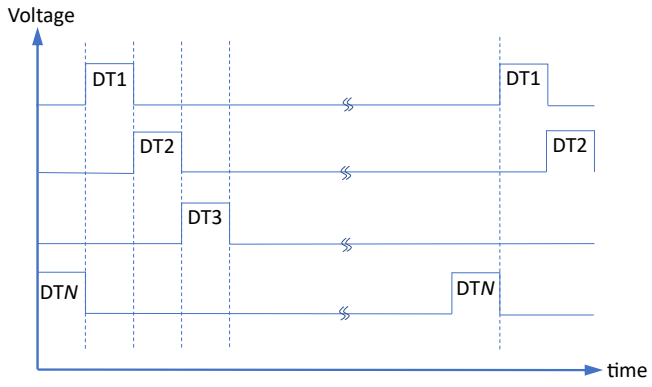



*Figure 2. Interleaved POL Converter Control Switch Timing*

Although there are design concerns regarding phase-to-phase current sharing and transient performance (which are beyond the scope of this discussion but addressed elsewhere), the multiphase interleaving of synchronous POL converters is a useful, reliable technique for providing the low voltage, high current requirements of the present generation of rad hard gate arrays and FPGAs and their associated infrastructure.

Beyond just the advantage of sharing load current to a common load, multi-phase interleaving allows for a smaller output capacitor to be used due to the fact that a smaller, higher frequency ripple current is present. Also, smaller phase inductors may be used due to the Io/N current handled by each phase. This relationship between the individual phase currents and the output filter capacitor current, for a four-phase interleaved POL circuit, is shown in Figure 3. In Figure 3 the **GREEN**, **BLUE**, **RED** and **LIGHT BLUE** traces are the individual phase currents, with the last three phase-shifted by 90 degrees from the previous phase. The **VIOLET** trace is the output capacitor current.

The apparent current ripple frequency for the current in the output capacitor is $f_S \cdot N$, where $f_S$ is the individual switching frequency of the interleaved POLs ($1/T_S$). This lower apparent frequency allows the designer to use a lower value, lower ESR capacitor as the output capacitor.

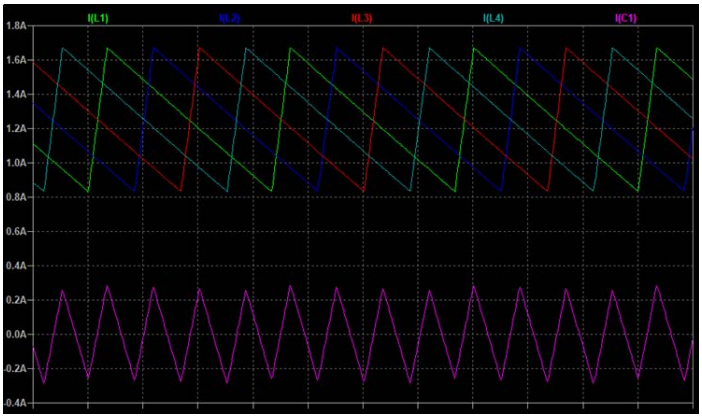



*Figure 3. Interleaved POL Phase Current and Output Capacitor Current*

## Practical Implementations of the Interleaved POL Converter

An interleaved POL configuration may be undertaken as a discrete design based on the GAM02 series, using individual PWM controller ICs to regulate the voltage of each phase. The most difficult part of such an undertaking is the design of the clock for each phase where each phase is phase-shifted by 360/N degrees. This is probably the greatest impediment to implementing the discrete approach, as there is a lot of rad-hard component hardware to deal with.

A more simplified method to implement the interleaved POL configuration with far less hardware is to utilize a rad-hard FPGA to generate the necessary phase-shifted PWM signals and to perform the requisite regulator function(s) for each phase. The drawback to this approach is the firmware necessary to do all these functions in synchronicity to the desired performance required.

The most attractive way to implement the interleaved POL function is to use a PWM controller purpose-designed to provide the necessary regulation and clock synchronization functions. Luckily there is a rad-hard controller IC that may be utilized that provides, along with the GAM02 half-bridge modules, a rad-hard, low parts count solution and implementation. The PWM controller in question is the Texas Instruments TPS7H5001-SP. It is a full-featured current-mode controller with complimentary outputs that also has the capability to provide signals for synchronous rectification. It can provide switching signals from 100kHz to 2MHz and it provides clock synchronization between two controllers such that four POL stages may be interleaved.

A single TPS7H5001-SP integrated circuit is capable of driving two phases of an interleaved POL. If two of these devices are interconnected as recommended in their data sheet, they are then capable of driving four phases of an interleaved POL. All the necessary dead times and phase-shifts are performed within the ICs.

Figure 4 shows a four-phase interleaved POL converter utilizing four FBS-GAM02 modules and two TPS7H5001-SP IC's. This configuration is capable of providing up to 40 A of load current.

It should be noted that the circuit shown in Figure 4 has been greatly simplified for clarity with regards to components utilized. Power supply bypass capacitors, voltage loop compensation components, current sense components, soft start and dead time-setting components have been omitted in lieu of the clarification of the power train. The selection and values of the components required by the TPS7H5001-SP device for a given desired operating frequency and output voltage may be found by referring to the device's data sheet.

Figure 5 shows a similar four-phase interleaved POL converter as that shown in Figure 4, except utilizing four FBS-GAM02-PSE modules and two TPS7H5001-SP IC's. This configuration is capable of providing up to 200A of load current. The minimum of 40A is noted in Figure 5 because this is the maximum current that the FBS-GAM02, a lower parts count/complexity solution, can provide.

In Figure 5 each switch function QCN (control switch) and QSN (synchronous switch) may be a single HEMT or multiple HEMTs from the EPC Space discrete HEMT product portfolio in parallel, depending upon the output voltage and duty cycle required. For example, if a 40 A total output current is required and the maximum $V_{DD}$ voltage is 20 V, the QCN and QSN could be adequately served by either the FBG04N30B or the EPC7019G, depending upon the gate drive capability and PCB layout area available. At the opposite end of the output current scale, if a 200 A total output current is required with the same maximum $V_{DD}$ voltage, then the same two transistors could be candidates, except in quantities of up to four devices in parallel for QCN and QSN, depending on the duty cycle. For example, at low duty cycles, switch QCN conducts for a relatively short time (DT), so one or two in parallel of the candidate HEMTs in parallel would be adequate. Conversely, switch QSN conducts for a longer period of time (1 – DT), so three or four of the candidates HEMTs in parallel might be required.

Regardless, depending upon the design requirements, for higher load currents, it is obvious that the interleaved POL converter topology along with the FBS-GAM02-PSE module offers the power designer a great deal of flexibility to "mix-and-match" properly-rated HEMTs alone or in parallel to suit the exact design requirements. And at load currents up to 40 A, the FBS-GAM02 offers the designer the lowest parts-count solution.

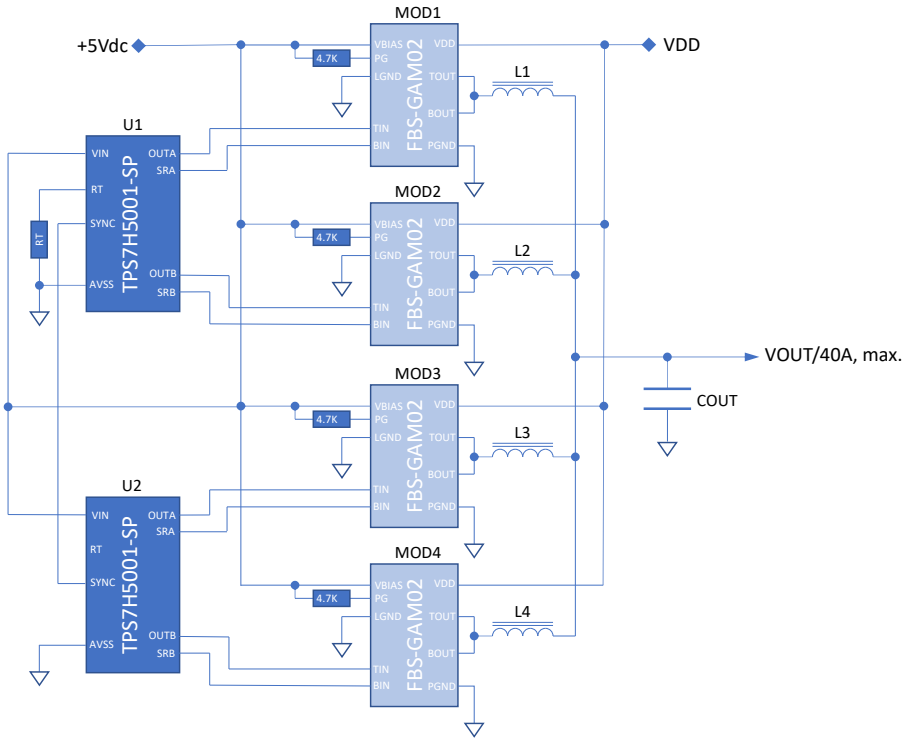



*Figure 4. FBS-GAM02 Four-Phase Interleaved POL Example*

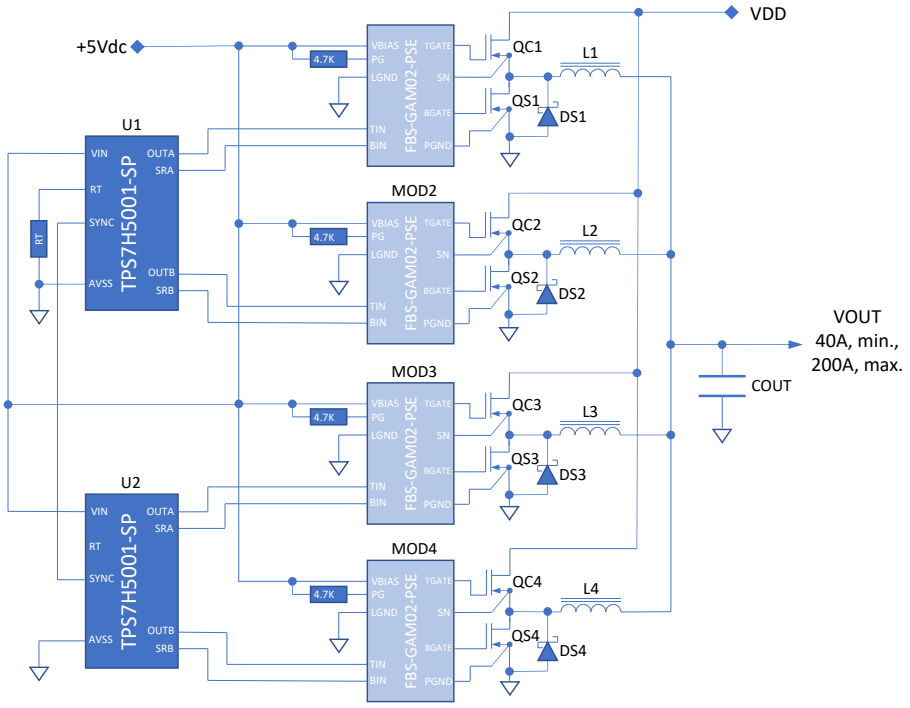



*Figure 5. FBS-GAM02-PSE Four-Phase Interleaved POL Example*

## Performance Results

An LTSPICE simulation was performed for a four-phase interleaved POL converter utilizing FBS-GAM02 modules. Efficiency performance data was collected for a 12 V-to-0.96 V converter operating at switching frequencies of 200 kHz and 500 kHz at load currents of 15, 20, 25, 30, 35 and 40 Adc. The inductors selected for the simulation were 2.75 µH with a DCR of 2 mΩ for 200 kHz operation and 1.5 µH with a DCR of 2 mΩ for 500 kHz operation. The output filter capacitance was chosen to be 5000 µF with an ESR of 30 mΩ for 200 kHz operation and 2000 µF with an ESR of 30 mΩ for 500 kHz operation. The results obtained from the simulation are plotted in Figure 6. It can be seen that at 200 kHz operation that the efficiency never drops below 90.5% and never drops below 84.5% for 500 kHz operation.

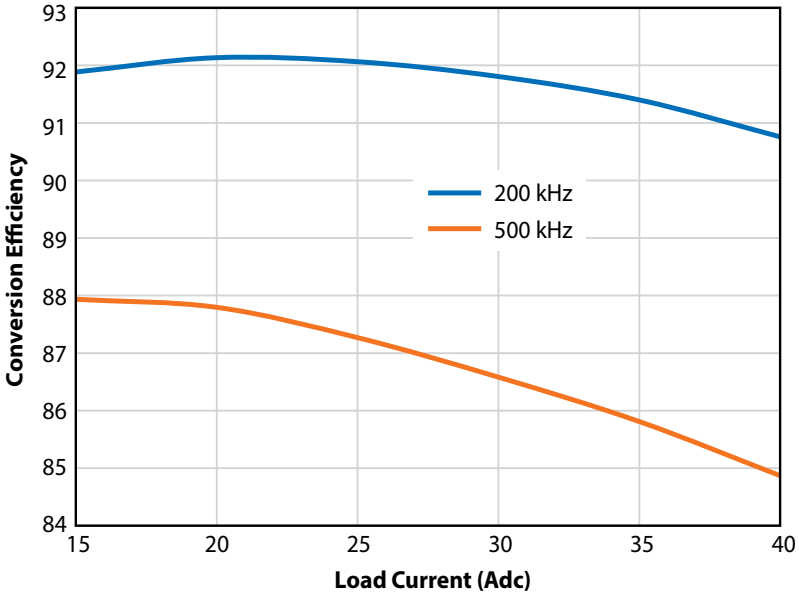



*Figure 6. FBS-GAM02 Four-Phase Interleaved POL Simulated Efficiency*

## Advantages and Other Considerations

The multi-phase interleaved converter can provide the end-user with benefits beyond increased power capability and high efficiency. Because each converter function is comprised of multiple equal power phases, these phases do not necessarily have to reside close to one-another in a power-designated area. The individual phases may be located close to the intended load in what convenient areas exist. The only caveat is that that sufficient power (input and output) and ground planes exist in the PCB copper etch stack up. Since each phase is regulating from a common power source ($V_{DD}$) to a common load ($V_{OUT}$), it is desirable to have a minimum plane resistance exist between phases. Otherwise, stability issues and load regulation problems and excessive output ripple may occur.

Since all the phases are equal power, it is advantageous to use a common PCB layout and component placement and consist of similar components - then each phase may be treated as a component, with only input and output power, ground and the input logic signals connecting to each phase block. This situation allows for true copy, cut and paste implementation of the POL power function.

## Conclusion and Summary

A method to increase the current capability of the FBS-GAM02 and FBS-GAM02-PSE (along with adjunct discrete power HEMTs) modules is proposed. Multiphase interleaving is introduced as this method. A practical implementation is shown using a commercially-available PWM controller that allows a four-phase interleaved converter to be provisioned with a minimum parts count. An LTSPICE simulation was performed to determine the efficiency of a four-phase interleaved POL converter using FBS-GAM02 modules for a 12 V-to-0.96 V conversion at 200 kHz and 500 kHz for a 40 A load. The results showed that high efficiency is obtained for an output current four times the capacity of an individual converter phase. The advantages of utilizing multiphase interleaving of individual identical phases are also discussed.

In conclusion it is proven that multiphase interleaving of FBS-GAM02 and FBS-GAM02-PSE modules can extend their useful current range by a factor of N, where N is the total number of interleaved phases. Thus, the FBS-GAM02 finds utility far in excess of its individual current rating of 10 A, and it allows the GAM02-PSE module (with appropriately-rated power HEMTs) satisfy load current requirements of 200 A and above.